plasma etch causes SiO_2 to etch preferentially compared to Si.

The silicon substrate **20** can be doped with impurities that pass through the narrow trenches to form the channel-stop layer **28**.

The device under fabrication is then subjected to a short (about 5 to 20 minutes) heat treatment at 850° C. to 950° C. in an oxygen-free environment, for example, in a helium or an argon atmosphere, or in an environment containing very little oxygen, to release the stress around the field oxide layer **25**, and eliminating most, preferably all, of the crystalline defects **26**. Meanwhile, the implanted impurities in the channel-stop layer are also electrically activated and re-distributed to form an even layer.

Referring now to FIG. **2E**, an insulating layer, such as silicon dioxide, polyimide, borophosphosilicate (BPSG) or the like, is deposited by, for example, CVD. All the narrow trenches within the field oxide layer **25** are filled, and a stress-free isolation layer **29** is obtained. Conventional procedures are then applied to sequentially strip off the nitride layer **23**, polysilicon layer **22** and pad oxide layer **21**, respectively. The silicon nodules **27** are also removed by this etch. For example, first the nitride layer is stripped using a conventional hot H_3PO_4 solution. Then the polysilicon layers are stripped by using a conventional KOH solution, or by using reactive ion etching. Finally, for stripping pad oxide, the device under fabrication is typically bathed in a solution containing HF. The device isolation is completed after these stripping steps.

Having described the invention in connection with a preferred embodiment, modification will now suggest itself to those skilled in the art. Thus the invention is not to be limited to the disclosed embodiment, except as required by the appended claims.

I claim:

1. A method of fabricating a stress-free isolation layer for semiconductor integrated circuits comprising the steps of:

(a) providing a silicon substrate;

(b) forming, sequentially, a) a pad oxide layer, b) a polysilicon layer, and c) a silicon nitride layer on said silicon substrate;

(c) etching said silicon nitride layer, said polysilicon layer, and said pad oxide layer to expose predetermined areas of said silicon substrate;

(d) etching said pre-determined areas of said silicon substrate to form at least one shallow trench;

(e) forming sidewall spacer nitride layers on side walls of said shallow trench in said silicon substrate;

(f) forming a field oxide layer that fills said shallow trench;

(g) etching designated areas of said field oxide layer to form at least one narrow trench in said field oxide layer;

(h) selectively ion implanting impurities through said at least one narrow trench into said silicon substrate;

(i) annealing said silicon substrate to release system stress, and to form a channel-stop layer in said silicon substrate;

(j) depositing an insulating layer to fill said at least one narrow trench in said field oxide layer to form the isolation layer; and

(k) stripping said silicon nitride layer, said polysilicon layer, and said pad oxide layer.

2. The method of claim **1** wherein the thickness of said pad oxide layer in step (b) is in the range of 80 to 500Å.

3. The method of claim **1** wherein the thickness of said polysilicon layer in step (b) is in the range of 100 to 2,000Å.

4. The method of claim **1** wherein the thickness of said silicon nitride layer in step (b) is in the range of 500 to 3,000Å.

5. The method of claim **1** wherein the depth of said at least one shallow trench in said silicon substrate in step (d) is in the range of 1,000 to 3,000Å.

6. The method of claim **1** wherein the thickness of said spacer nitride layer in step (e) is in the range of 100 to 1000Å.

7. The method of claim **1** wherein said step (g) further comprises the following steps:

(g1) forming a hot metal-silicon alloy layer with a thickness in the range of 5,000 to 20,000Å on the exposed surface of said field oxide layer and said silicon nitride layer and allowing the alloy layer to cool;

(g2) etching said metal alloy layer thereby forming a plurality of silicon nodules having sizes in the range of 500 to 3,000Å.

(g3) etching said filed oxide layer by utilizing said silicon nodules as mask and said polysilicon as etching-stop layer to form at least one narrow trench in said field oxide layer.

8. The method of claim **1** wherein the insulating layer in step (j) is a silicon dioxide layer.

9. The method of claim **1** wherein the insulating layer in step (j) is a polyimide layer.

10. The method of claim **1** wherein the insulating layer in step (j) is a BPSG layer.

11. The method of claim **7** wherein said metal alloy layer is aluminum-silicon alloy.

12. The method of claim **11** wherein the silicon content of the alloy is in the range of 1 to 4%.

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